Notice of Allowability	Application No.	Applicant(s)	
	10/751,529	ISHIKAWA ET AL.	
	Examiner	Art Unit	
	Nitin Patel	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *12/21/2006*.

2. ☒ The allowed claim(s) is/are *1-4,6-13 Now renumbered 1-12 respectively*.

3. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☒ All b) ☐ Some* c) ☐ None of the:
      1. ☒ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

NITIN I. PATEL
PRIMARY EXAMINER

REASON FOR ALLOWANCE

1. Claims 1-4,6-13 are allowed. Claim 5 has been cancelled.

2. The following is an examiner's statement of reason for allowance:

The prior art fails to teach or suggest A liquid crystal display device having a plurality of data signal lines, a plurality of gate signal lines disposed intersection to the data signal lines, pixel transistors disposed at intersections of the data signal lines and the gate signal lines, and capacitors disposed at the intersections, the pixel transistors each having a control electrode, an input electrode, and an output electrode, at the intersections, the control electrodes of the pixel transistors being connected to the respective gate signal lines, the input electrodes of the pixel transistors being connected to the respective data signal lines, the output electrodes of the pixel transistors being connected to the respective capacitors, the liquid crystal display device comprising: **comparing means for comparing voltages of output signals from at least two data signals line.**

The prior art fails to teach or suggest a liquid crystal display device having a plurality of data signal lines, a plurality of gate signal lines disposed intersection to the data signal lines, pixel transistors disposed at intersections of the data signal lines and the gate signal lines, and capacitors disposed at the intersections, the pixel transistors each having a control electrode, an input electrode, and an output electrode, at the intersections, the control electrodes of the pixel transistors being connected to the respective gate signal lines, the input electrodes of the pixel transistors being connected to the respective data signal lines, the output electrodes of the pixel transistors being

connected to the respective capacitors, **the liquid crystal display device comprising: means disposed at intervals of two of the data signal lines for comparing voltages of the two data signal lines** as claimed in claim 6.

The prior art fails to teach or suggest a liquid crystal display device having a plurality of data signal lines, a plurality of gate signal lines disposed intersection to the data signal lines, pixel transistors disposed at intersections of the data signal lines and the gate signal lines, and capacitors disposed at the intersections, the pixel transistors each having a control electrode, an input electrode, and an output electrode, at the intersections, the control electrodes of the pixel transistors being connected to the respective gate signal lines, the input electrodes of the pixel transistors being connected to the respective data signal lines, the output electrodes of the pixel transistors being connected to the respective capacitors, the liquid crystal display device comprising: a **plurality of auxiliary data signal lines disposed corresponding to the data signal lines and connected to the output electrodes of the respective pixel transistors; and calculating means connected to one of the auxiliary data signal lines and one of the gate signal lines** as claimed in claim 9.

The prior art fails to teach or suggest a method for inspecting a liquid crystal display device having a plurality of data signal lines, a plurality of gate signal lines disposed intersection to the data signal lines, pixel transistors disposed at intersections of the data signal lines and the gate signal lines, and capacitors disposed at the intersections, the pixel transistors each having a control electrode, an input electrode, and an output electrode, at the intersections, the control electrodes of the pixel

transistors being connected to the respective gate signal lines, the input electrodes of the pixel transistors being connected to the respective data signal lines, the output electrodes of the pixel transistors being connected to the respective capacitors, the method comprising the steps of: **supplying two predetermined different voltages to two adjacent data signal lines and storing the two predetermined different voltages to capacitors connected to the two signal lines through the respective pixel transistors; and comparing voltages that are read from the capacitors to the two data signal lines** as claimed in claim 10.

The prior art fails to teach or suggest a method for inspecting a liquid crystal display device having a plurality of data signal lines, a plurality of gate signal lines disposed intersection to the data signal lines, pixel transistors disposed at intersections of the data signal lines and the gate signal lines, and capacitors disposed at the intersections, the pixel transistors each having a control electrode, an input electrode, and an output electrode, at the intersections, the control electrodes of the pixel transistors being connected to the respective gate signal lines, the input electrodes of the pixel transistors being connected to the respective data signal lines, the output electrodes of the pixel transistors being connected to the respective capacitors, the method comprising the steps of: **supplying different voltages to two data signal lines and storing the two different voltages to the capacitors through the respective pixel transistors connected to the two data signal lines; pre-charging a reference potential to all the data signal lines and reading voltages stored in the**

capacitors to the two data signal lines; and comparing the voltages of the two data signal lines as claimed in claim 11.

The prior art fails to teach or suggest a method for inspecting a liquid crystal display device having a plurality of data signal lines, a plurality of gate signal lines disposed intersection to the data signal lines, pixel transistors disposed at intersections of the data signal lines and the gate signal lines, and capacitors disposed at the intersections, the pixel transistors each having a control electrode, an input electrode, and an output electrode, at the intersections, the control electrodes of the pixel transistors being connected to the respective gate signal lines, the input electrodes of the pixel transistors being connected to the respective data signal lines, the output electrodes of the pixel transistors being connected to the respective capacitors, the method comprising the steps of: **supplying different voltages to two data signal lines and storing the two different voltages to the capacitor through the respective pixel transistors connected to the two data signal lines; for each gate signal line reading the voltages stored in the capacitors at the intersections of the gate signal line and the two data signal lines; comparing the voltages that are read with a comparing means and detecting defective pixels based upon the result of the comparison** as claimed in claim 13.

3. Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

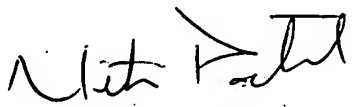
Conclusion

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nitin Patel whose telephone number is 571-272-7677. The examiner can normally be reached on 8:00-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bipin H. Shalwala can be reached on 571-272-7681. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Nitin Patel
Primary Examiner
Art Unit 2629



NITIN I. PATEL
PRIMARY EXAMINER